

## **Introduction**

As mentioned in previous documents, a “Digital Picture Box” is being designed that acts essentially as a buffer between a personal computer storing digital photographs and a VGA compatible display. This system permits individuals to convert old VGA compatible devices (CRT, LCD monitors, etc) into “Digital Picture Frames.” The system also has other practical uses...for instance, displaying images (perhaps of lecture slides for a class) on a VGA-compatible projector.

The system works basically as follows: JPEG images are decoded and then transferred to a Rabbit 3000 Core Module’s RJ-45 port. Once received, the Rabbit interfaces with an Epson graphics controller which is responsible for generating the appropriate VGA signals. The Epson also interfaces with a 256K x 16 EDO DRAM memory chip that is used as a “framebuffer” to store a particular image. The system operates using a standard unregulated 9 VDC wall wart, which is respectively converted to +5V and +3.3V via low-dropout regulators. The digital picture box also has a built-in IR receiver/decoder which permits the use of an IR remote control, allowing one to place the VGA device and picture box in a relatively inaccessible location. Finally, there are also status LED’s along with pushbuttons to control the system directly from the box.

In order for the aforementioned components to work properly together, careful attention must be given to the printed circuit board layout. The fact that the Epson contains a DAC, for instance, affects layout strategies considerably. The remainder of this abstract focuses on what exactly these concerns are as well as the approaches used to overcome them.

## **PCB Layout Design Considerations**

As mentioned in the Motorola Semiconductor Application Note, one of the most important concerns for layout is the power system. Specifically, keeping components that are sensitive to noise (analog devices, for instance) separate from those that create noise (ie, high power devices, fast switching devices, etc). In the digital picture box’s case there are two primary components that need to be kept separate from each other: the digital part of the board and the analog DAC present on the Epson graphics controller. This separation is achieved through a couple of ways. First, the DAC has a separate LDO for

its power source. This, coupled with the separation of DAC and digital ground via a ferrite bead, eliminates the ability of digital noise to be directly introduced into the DAC.

At this point there are still indirect concerns; namely, coupling through magnetic radiation (ie, nearby digital components and their traces affecting the DAC through EMF coupling). A few steps were taken to prevent this. First, all analog components were kept a notable distance from other digital components. Second, in most cases traces that had to run over or under a trace relating to the analog part of the system were run in a manner that made them perpendicular to the analog traces, thus reducing the EMF coupling. Finally, the +5V LDO and related components were placed on the opposite side of the board, in an attempt to keep the relatively higher power aspects of the system as far away from the DAC and analog components as possible.

In terms of the general board layout, numerous methods were employed to reduce EMI and related noise. For starters, traces run on the bottom layer of the board were done from top-to-bottom in most cases whereas traces run on the top layer were done from left-to-right. Again, as mentioned above this was done to reduce the EMF coupling and induced noise between traces. The notable exception to this is the region surrounding the Epson controller. Given the roughly 6.5mil sized pads and relatively small spacing constraints, many of the traces on the top layer ended up running from top-to-bottom. Next, decoupling capacitors were placed as close to the IC's as possible to reduce noise and compensate for current spikes related to unexpectedly high transistor switching. Decoupling capacitors were generally placed directly beneath the main IC's (which consist of the Epson controller, the EDO DRAM chip, the IR controller, and LDO regulators). Finally, per the Motorola document's recommendations, the 25.125MHz crystal was also placed as close to the Epson (the only externally clocked device onboard) as possible. Clock traces were kept as short as possible and any inductive loops were avoided at all costs.

EMI aside, component placing was also influenced by actual components' purposes. The VGA connector was placed on a board edge, as would be expected. The IR receiver was also placed on an edge in addition to the push buttons and LED's. The rabbit's built-in Ethernet jack is not on an edge for routing simplicity. Instead, we intend to connect an "extender dangle" to the rabbit and run it outside of the actual box.

Priority was also taken into consideration during the routing process. The Epson, being the smallest and most complicated chip, was routed first; followed by the DRAM, the Address and Control PLD's, the Rabbit microcontroller, LED's and Pushbuttons, "Analog" components, "IR" components, and finally the debug headers.

Most trace sizes were 12 mils with the exception of traces related to the Epson. Larger trace sizes were attempted for power, but generally caused problems in most areas. As such, 12 mils is used consistently throughout the board in most cases. 90 degree angles were also avoided whenever possible.

All of these considerations and other minor ones were combined and utilized in what hopefully turns out to be a successful attempt to create a usable and environmentally-friendly PCB layout.

Following is a copy of the bottom and top layers of the PCB as well as routing statistics, an updated BOM, an updated schematic and its related DRC report. References to spec sheets and other documents are located last. Note that many of the specs for creating custom footprints were gathered from these documents.

## References

### Motorola Semiconductor Application Note AP1259

<http://shay.ecn.purdue.edu/~dsml/ece477/Homework/Spr2004/AN1259.pdf>

### Rabbit 3000 Core Module

[http://shay.ecn.purdue.edu/~477grp12/datasheets/rabbit3000\\_core\\_manual.pdf](http://shay.ecn.purdue.edu/~477grp12/datasheets/rabbit3000_core_manual.pdf)

### Epson Graphics Controller

[http://shay.ecn.purdue.edu/~477grp12/datasheets/epson\\_manual.pdf](http://shay.ecn.purdue.edu/~477grp12/datasheets/epson_manual.pdf)

### Dropout Voltage Regulators

#### 3.3V

<http://focus.ti.com/lit/ds/symlink/reg103-33.pdf>

#### 5V

<http://focus.ti.com/lit/ds/symlink/reg103-5.pdf>

### PLD

#### 26V12

[http://www.vantis.com/lit/docs/datasheets/pal\\_gal/26v12.pdf](http://www.vantis.com/lit/docs/datasheets/pal_gal/26v12.pdf)

#### 16V8

[http://www.vantis.com/lit/docs/datasheets/pal\\_gal/16v8.pdf](http://www.vantis.com/lit/docs/datasheets/pal_gal/16v8.pdf)

### IR

#### Detector

[http://shay.ecn.purdue.edu/~477grp12/datasheets/sharp\\_ir\\_detector\\_data.pdf](http://shay.ecn.purdue.edu/~477grp12/datasheets/sharp_ir_detector_data.pdf)

#### Decoder

[http://shay.ecn.purdue.edu/~477grp12/datasheets/rentron\\_ir\\_decoder.pdf](http://shay.ecn.purdue.edu/~477grp12/datasheets/rentron_ir_decoder.pdf)

### DRAM

<http://www.issi.com/pdf/41xx16256.pdf>

### Crystal Oscillator

[http://www.eea.epson.com/go/Prod\\_Admin/Categories/EEA/QD/Crystal\\_Oscillators/all\\_oscillators/go/Resources/TestC2/SG8002DB](http://www.eea.epson.com/go/Prod_Admin/Categories/EEA/QD/Crystal_Oscillators/all_oscillators/go/Resources/TestC2/SG8002DB)