

# DMOS

## 500mA Low-Dropout Regulator

### FEATURES

- **NEW DMOS TOPOLOGY:**  
Ultra Low Dropout Voltage:  
115mV Typ at 500mA and 3.3V Output  
Output Capacitor NOT Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE:** 33 $\mu$ Vrms
- **HIGH ACCURACY:**  $\pm$ 2% max
- **HIGH EFFICIENCY:**  
 $I_{GND} = 1\text{mA}$  at  $I_{OUT} = 500\text{mA}$   
Not Enabled:  $I_{GND} = 0.5\mu\text{A}$
- **2.5V, 2.7V, 3.0V, 3.3V, 5.0V, AND ADJUSTABLE OUTPUT VERSIONS**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **OUTPUT VOLTAGE ERROR INDICATOR<sup>(1)</sup>**
- **SMALL SURFACE-MOUNT PACKAGES:**  
SOT223-5, DDPAK-5, SO-8

### APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

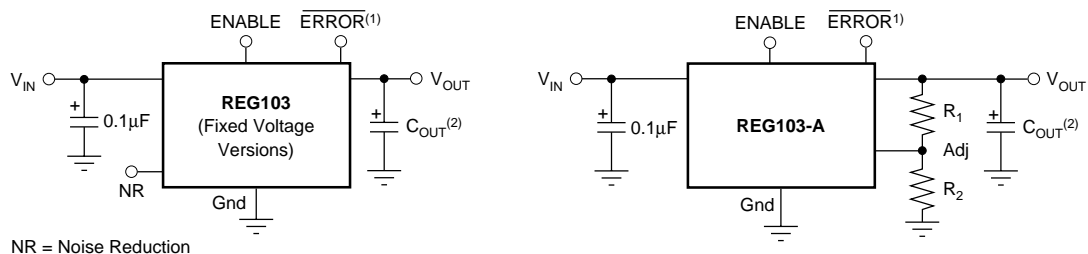
### DESCRIPTION

The REG103 is a family of low-noise, low-dropout, linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 115mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1 $\mu$ F.

Typical ground pin current is only 1mA (at  $I_{OUT} = 500\text{mA}$ ) and drops to 0.5 $\mu\text{A}$  in *not enabled* mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG103 has very low output noise (typically 33 $\mu\text{Vrms}$  for  $V_{OUT} = 3.3\text{V}$  with  $C_{NR} = 0.01\mu\text{F}$ ), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ).

The SO-8 version of the REG103 has an  $\overline{\text{ERROR}}$  pin that provides a *power good* flag, indicating the regulator is in regulation. The REG103 is well protected—internal circuitry provides a current limit that protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. In addition to the SO-8 package, the REG103 is also available in the DDPAK and the SOT223-5.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Input Voltage, $V_{IN}$ .....	-0.3V to 16V
Enable Input .....	-0.3V to $V_{IN}$
Error Flag Output .....	-0.3V to 6V
Error Flag Current .....	2mA
Output Short-Circuit Duration .....	Indefinite
Operating Temperature Range .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	-55°C to +150°C
Lead Temperature (soldering, 3s, SO-8, SOT, and DDPAK) .....	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
<b>5V Output</b>						
REG103FA-5	DDPAK-5	KTT	-40°C to +85°C	REG103FA-5.0	REG103FA-5KTTT	Tape and Reel, 50
"	"	"	"	"	REG103FA-5/500	Tape and Reel, 500
REG103UA-5	SO-8	D	-40°C to +85°C	REG103U50	REG103UA-5	Rails, 100
"	"	"	"	"	REG103UA-5/2K5	Tape and Reel, 2500
REG103GA-5	SOT223-5	DCQ	-40°C to +85°C	R103G50	REG103GA-5	Rails, 78
"	"	"	"	"	REG103GA-5/2K5	Tape and Reel, 2500
<b>3.3V Output</b>						
REG103FA-3.3	DDPAK-5	KTT	-40°C to +85°C	REG103FA-3.3	REG103FA-3.3KTTT	Tape and Reel, 50
"	"	"	"	"	REG103FA-3.3/500	Tape and Reel, 500
REG103UA-3.3	SO-8	D	-40°C to +85°C	REG103UA4	REG103UA-3.3	Rails, 100
"	"	"	"	"	REG103UA-3.3/2K5	Tape and Reel, 2500
REG103GA-3.3	SOT223-5	DCQ	-40°C to +85°C	R103G33	REG103GA-3.3	Rails, 78
"	"	"	"	"	REG103GA-3.3/2K5	Tape and Reel, 2500
<b>3.0V Output</b>						
REG103FA-3	DDPAK-5	KTT	-40°C to +85°C	REG103FA-3.0	REG103FA-3KTTT	Tape and Reel, 50
"	"	"	"	"	REG103FA-3/500	Tape and Reel, 500
REG103UA-3	SO-8	D	-40°C to +85°C	REG103U30	REG103UA-3	Rails, 100
"	"	"	"	"	REG103UA-3/2K5	Tape and Reel, 2500
REG103GA-3	SOT223-5	DCQ	-40°C to +85°C	R103G30	REG103GA-3	Rails, 78
"	"	"	"	"	REG103GA-3/2K5	Tape and Reel, 2500
<b>2.7V Output</b>						
REG103FA-2.7	DDPAK-5	KTT	-40°C to +85°C	REG103FA-2.7	REG103FA-2.7KTTT	Tape and Reel, 50
"	"	"	"	"	REG103FA-2.7/500	Tape and Reel, 500
REG103UA-2.7	SO-8	D	-40°C to +85°C	REG103U27	REG103UA-2.7	Rails, 100
"	"	"	"	"	REG103UA-2.7/2K5	Tape and Reel, 2500
REG103GA-2.7	SOT223-5	DCQ	-40°C to +85°C	R103G27	REG103GA-2.7	Rails, 78
"	"	"	"	"	REG103GA-2.7/2K5	Tape and Reel, 2500
<b>2.5V Output</b>						
REG103FA-2.5	DDPAK-5	KTT	-40°C to +85°C	REG103FA-2.5	REG103FA-2.5KTTT	Tape and Reel, 50
"	"	"	"	"	REG103FA-2.5/500	Tape and Reel, 500
REG103UA-2.5	SO-8	D	-40°C to +85°C	REG103U25	REG103UA-2.5	Rails, 100
"	"	"	"	"	REG103UA-2.5/2K5	Tape and Reel, 2500
REG103GA-2.5	SOT223-5	DCQ	-40°C to +85°C	R103G25	REG103GA-2.5	Rails, 78
"	"	"	"	"	REG103GA-2.5/2K5	Tape and Reel, 2500
<b>Adjustable Output</b>						
REG103FA-A	DDPAK-5	KTT	-40°C to +85°C	REG103FA-A	REG103FA-AKTTT	Tape and Reel, 50
"	"	"	"	"	REG103FA-A/500	Tape and Reel, 500
REG103UA-A	SO-8	D	-40°C to +85°C	REG103UA	REG103UA-A	Rails, 100
"	"	"	"	"	REG103UA-A/2K5	Tape and Reel, 2500
REG103GA-A	SOT223-5	DCQ	-40°C to +85°C	R103GA	REG103GA-A	Rails, 78
"	"	"	"	"	REG103GA-A/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, refer to our web site at [www.ti.com](http://www.ti.com).

# ELECTRICAL CHARACTERISTICS

**Boldface limits apply over the specified temperature range,  $T_J = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .**

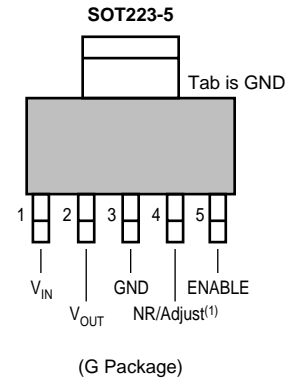
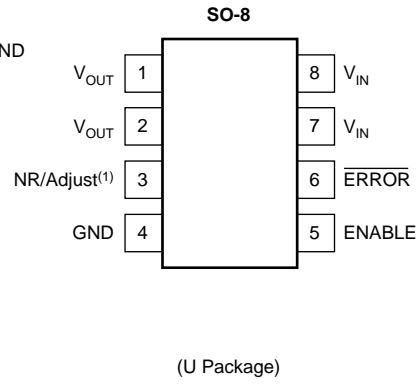
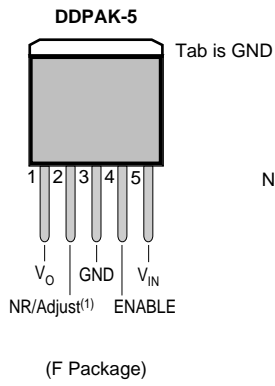
At  $T_J = +25^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$  ( $V_{OUT} = 3.0\text{V}$  for REG103-A),  $V_{ENABLE} = 2\text{V}$ ,  $I_{OUT} = 10\text{mA}$ ,  $C_{NR} = 0.01\mu\text{F}$ , and  $C_{OUT} = 0.1\mu\text{F}^{(1)}$ , unless otherwise noted.

PARAMETER	CONDITION	REG103GA, UA, FA			UNITS
		MIN	TYP	MAX	
<b>OUTPUT VOLTAGE</b>					
Output Voltage Range	$V_{OUT}$				V
REG103-2.5			2.5		V
REG103-2.7			2.7		V
REG103-3.0			3.0		V
REG103-3.3			3.3		V
REG103-5			5		V
REG103-A					V
Reference Voltage	$V_{REF}$		1.295	5.5	V
Adjust Pin Current	$I_{ADJ}$		0.2	1	$\mu\text{A}$
Accuracy			$\pm 0.5$	$\pm 2$	%
<b><math>T_J = -40^{\circ}\text{C}</math> to <math>+85^{\circ}\text{C}</math></b>				<b><math>\pm 2.8</math></b>	%
<b>vs Temperature</b>	$dV_{OUT}/dT$	<b><math>T_J = -40^{\circ}\text{C}</math> to <math>+85^{\circ}\text{C}</math></b>	<b>70</b>		ppm/ $^{\circ}\text{C}$
<b>vs Line and Load</b>		$I_{OUT} = 10\text{mA}$ to $500\text{mA}$ , $V_{IN} = (V_{OUT} + 0.7\text{V})$ to $15\text{V}$	$\pm 0.5$	$\pm 2.5$	%
<b><math>T_J = -40^{\circ}\text{C}</math> to <math>+85^{\circ}\text{C}</math></b>		<b><math>V_{IN} = (V_{OUT} + 0.9\text{V})</math> to <math>15\text{V}</math></b>		<b><math>\pm 3.5</math></b>	%
<b>DC DROPOUT VOLTAGE<sup>(2, 3)</sup></b>	$V_{DROP}$				
For all models except 5V		$I_{OUT} = 10\text{mA}$	3	25	mV
For 5V model		$I_{OUT} = 500\text{mA}$	115	200	mV
For all models except 5V		$I_{OUT} = 500\text{mA}$	160	250	mV
$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		$I_{OUT} = 500\text{mA}$		<b>230</b>	mV
For 5V models		$I_{OUT} = 500\text{mA}$		<b>280</b>	mV
$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$					
<b>VOLTAGE NOISE</b>	$V_n$				
$f = 10\text{Hz}$ to $100\text{kHz}$		$C_{NR} = 0$ , $C_{OUT} = 0$			
Without $C_{NR}$ (all models)		$C_{NR} = 0.01\mu\text{F}$ , $C_{OUT} = 10\mu\text{F}$			
With $C_{NR}$ (all fixed voltage models)				$30\mu\text{Vrms}/\text{V} \cdot V_{OUT}$	$\mu\text{Vrms}$
				$10\mu\text{Vrms}/\text{V} \cdot V_{OUT}$	$\mu\text{Vrms}$
<b>OUTPUT CURRENT</b>	$I_{CL}$				
Current Limit <sup>(4)</sup>			550	700	950
$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			<b>500</b>		<b>1000</b>
					mA
					mA
<b>RIPPLE REJECTION</b>					
$f = 120\text{Hz}$				65	dB
<b>ENABLE CONTROL</b>					
$V_{ENABLE}$ HIGH (output enabled)	$V_{ENABLE}$		2		V
$V_{ENABLE}$ LOW (output disabled)			-0.2		V
$I_{ENABLE}$ HIGH (output enabled)	$I_{ENABLE}$	$V_{ENABLE} = 2\text{V}$ to $V_{IN}$ , $V_{IN} = 2.1\text{V}$ to $6.5^{(5)}$		1	100
$I_{ENABLE}$ LOW (output disabled)		$V_{ENABLE} = 0\text{V}$ to $0.5\text{V}$		2	100
Output Disable Time				50	$\mu\text{s}$
Output Enable Soft Start Time				1.5	ms
<b>ERROR FLAG<sup>(6)</sup></b>					
Current, Logic HIGH (open drain)—Normal Operation		$V_{IN} = V_{ERROR} = V_{OUT} + 1\text{V}$		0.1	10
Voltage, Logic LOW—On Error		Sinking $500\mu\text{A}$		0.2	0.4
					$\mu\text{A}$
					V
<b>THERMAL SHUTDOWN</b>					
Junction Temperature				150	$^{\circ}\text{C}$
Shutdown				130	$^{\circ}\text{C}$
Reset from Shutdown					
<b>GROUND PIN CURRENT</b>					
Ground Pin Current	$I_{GND}$	$I_{OUT} = 10\text{mA}$		0.5	0.7
		$I_{OUT} = 500\text{mA}$		1	1.3
ENABLE Pin LOW		$V_{ENABLE} \leq 0.5\text{V}$		0.5	
					mA
					mA
					$\mu\text{A}$
<b>INPUT VOLTAGE</b>	$V_{IN}$				
Operating Input Voltage Range <sup>(7)</sup>		$V_{IN} > 2.7\text{V}$	2.1		15
Specified Input Voltage Range		$V_{IN} > 2.9\text{V}$	$V_{OUT} + 0.7$		15
$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			<b><math>V_{OUT} + 0.9</math></b>		<b>15</b>
					V
					V
					V
<b>TEMPERATURE RANGE</b>	$T_J$				
Specified Range			-40		+85
Operating Range			-55		+125
Storage Range			-65		+150
Thermal Resistance					
DDPAK-5 Surface-Mount	$\theta_{JC}$	Junction-to-Case		4	$^{\circ}\text{C}/\text{W}$
SO-8 Surface-Mount	$\theta_{JA}$	Junction-to-Ambient		150	$^{\circ}\text{C}/\text{W}$
SOT223-5 Surface-Mount	$\theta_{JC}$	Junction-to-Case		15	$^{\circ}\text{C}/\text{W}$

NOTES: (1) The REG103 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection. (2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at  $V_{IN} = V_{OUT} + 1\text{V}$  at fixed load. (3) Not applicable for  $V_{OUT}$  less than 2.7V. (4) Current limit is the output current that produces a 10% change in output voltage from  $V_{IN} = V_{OUT} + 1\text{V}$  and  $I_{OUT} = 10\text{mA}$ . (5) For  $V_{IN} > 6.5\text{V}$ , see typical characteristic " $V_{ENABLE}$  vs  $I_{ENABLE}$ ." (6) Logic low indicates out-of-regulation condition by approximately 10%, or thermal shutdown. (7) The REG103 no longer regulates when  $V_{IN} < V_{OUT} + V_{DROP(MAX)}$ . In drop-out or when the input voltage is between 2.7V and 2.1V, the impedance from  $V_{IN}$  to  $V_{OUT}$  is typically less than  $1\Omega$  at  $T_J = +25^{\circ}\text{C}$ . See typical characteristic.

# PIN CONFIGURATIONS

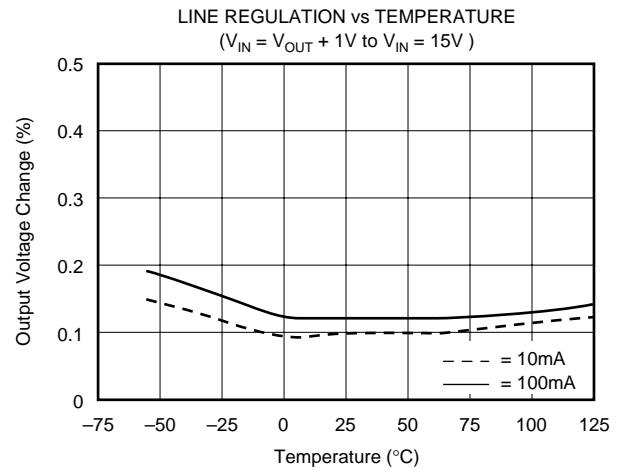
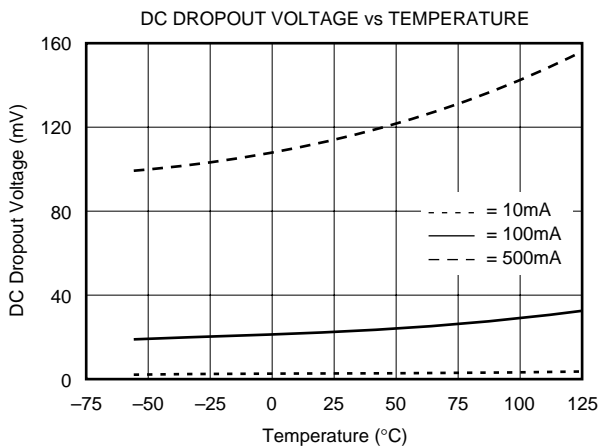
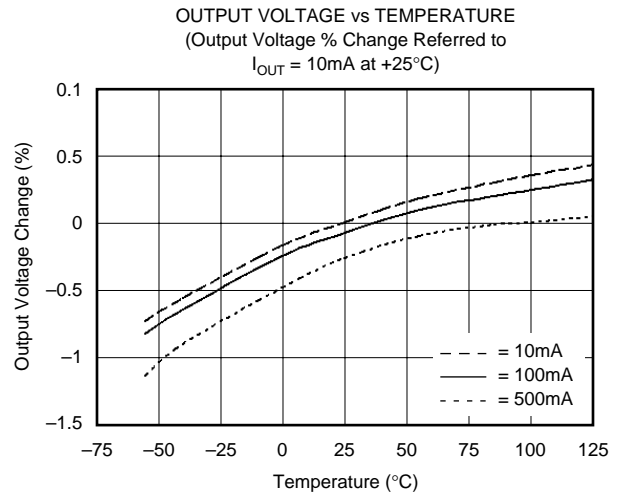
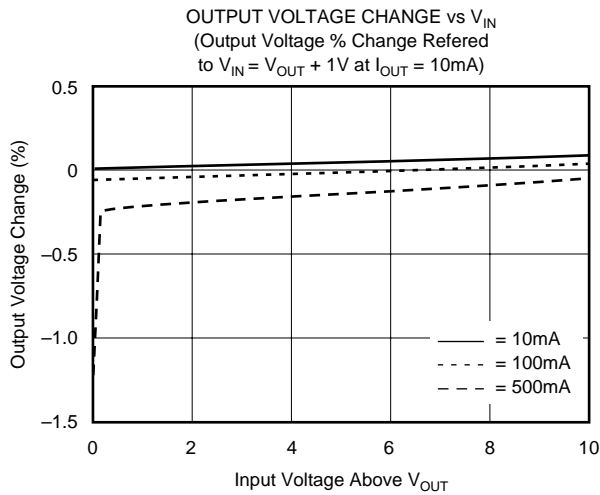
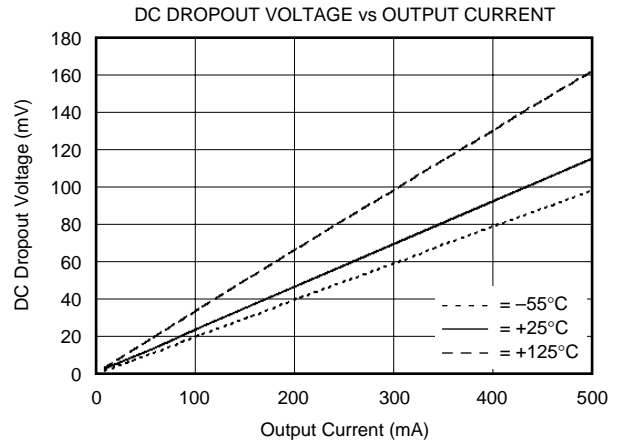
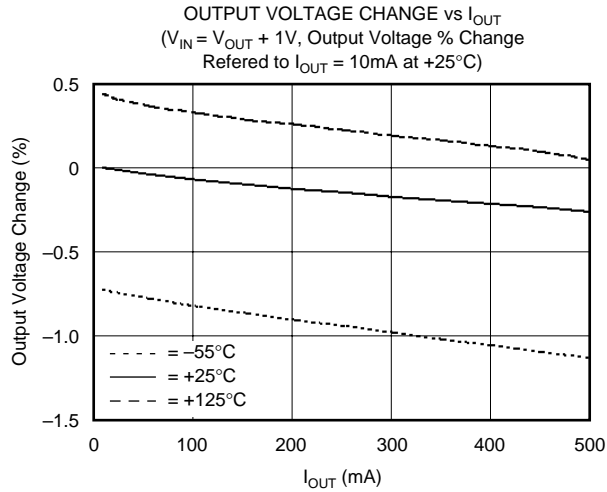
Top View



NOTE: (1) For REG103A-A: voltage setting resistor pin.  
All other models: noise reduction capacitor pin.

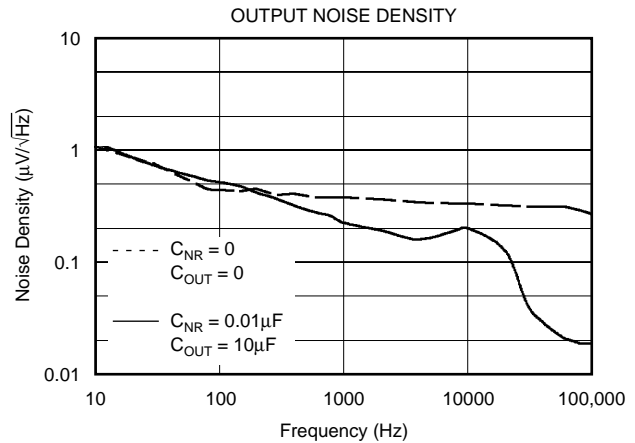
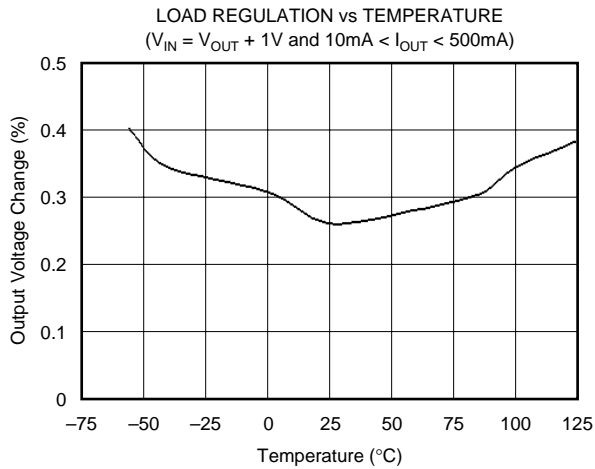
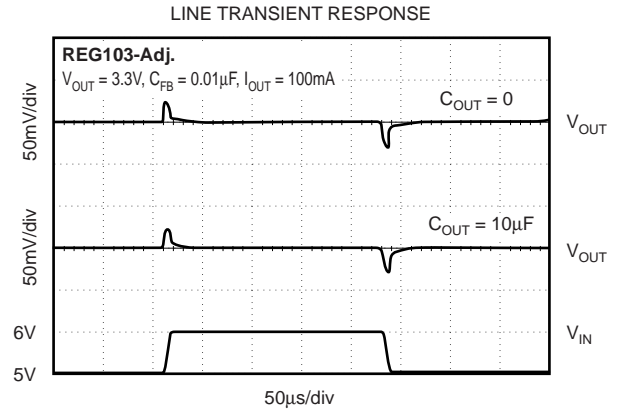
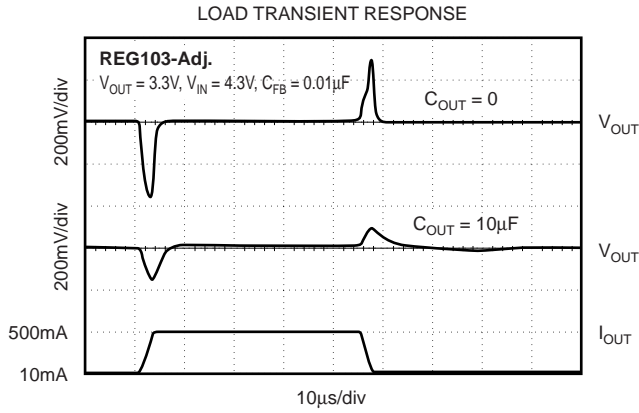
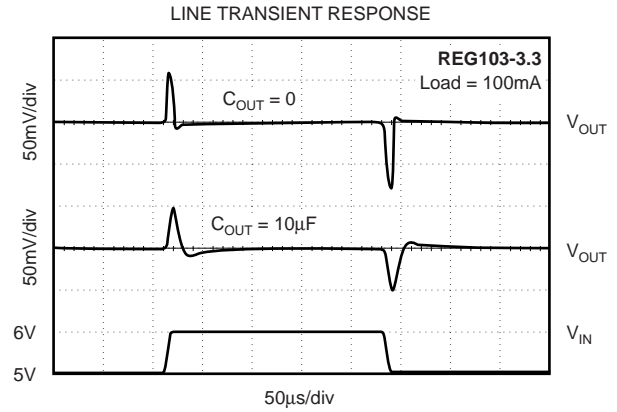
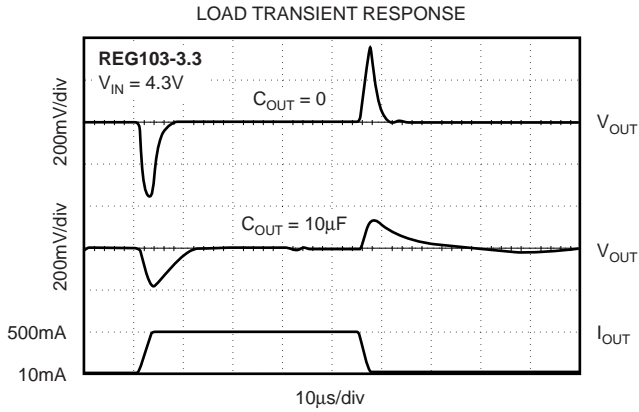
# TYPICAL CHARACTERISTICS

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 2\text{V}$ , unless otherwise noted.



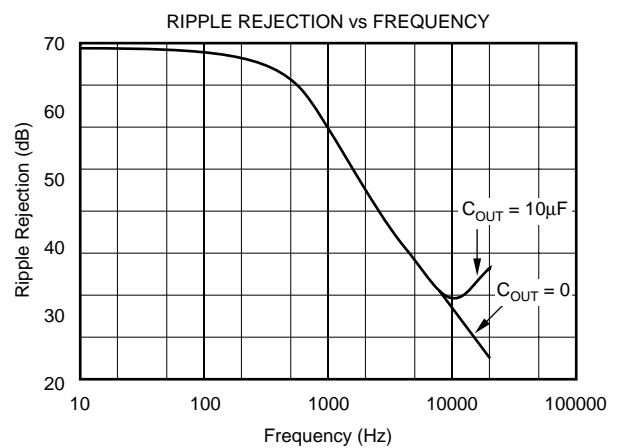
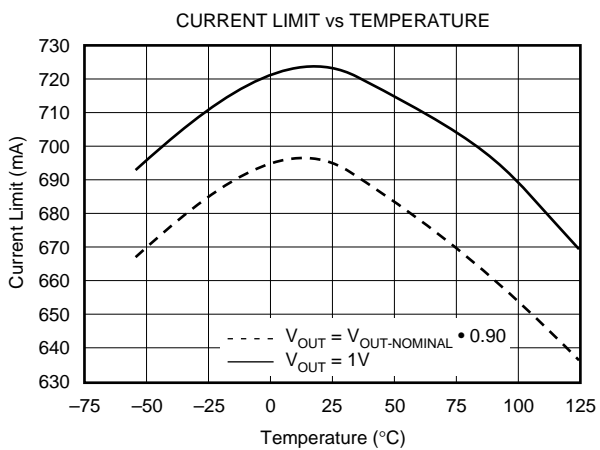
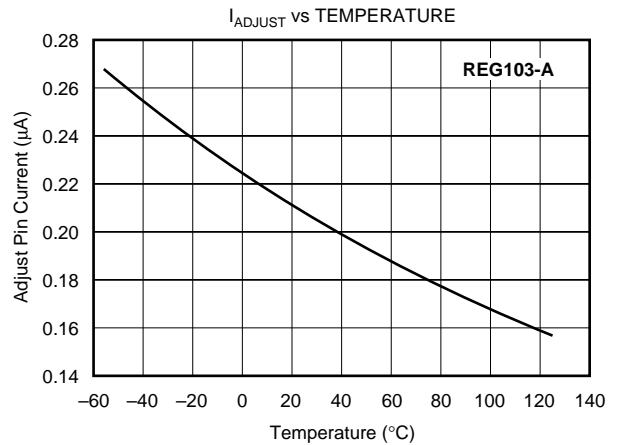
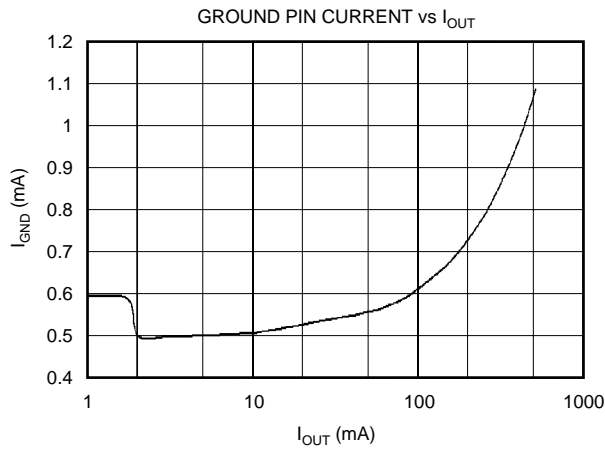
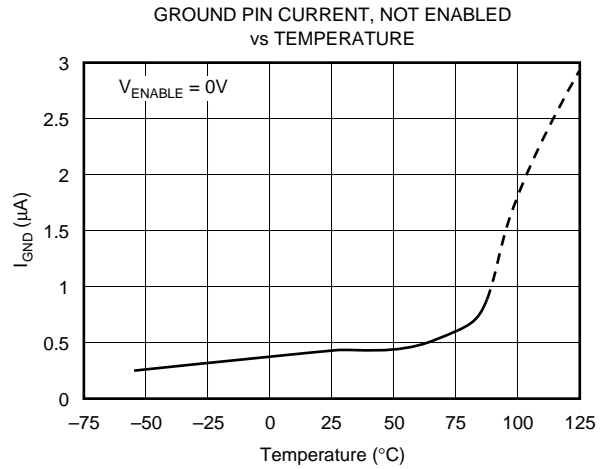
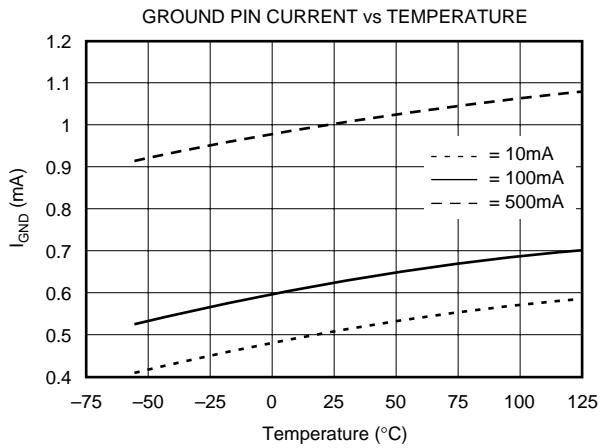
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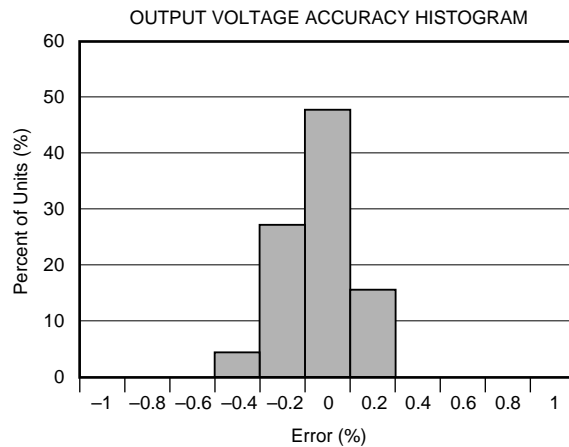
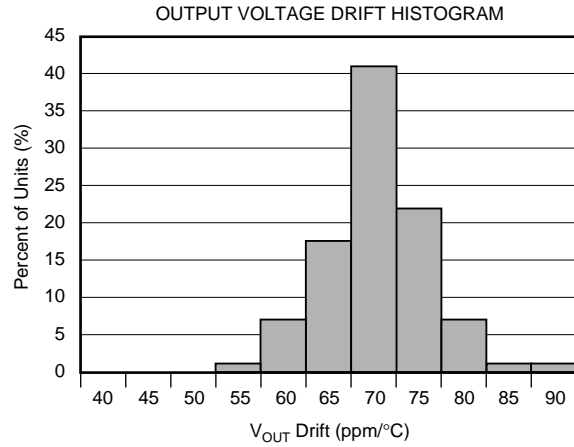
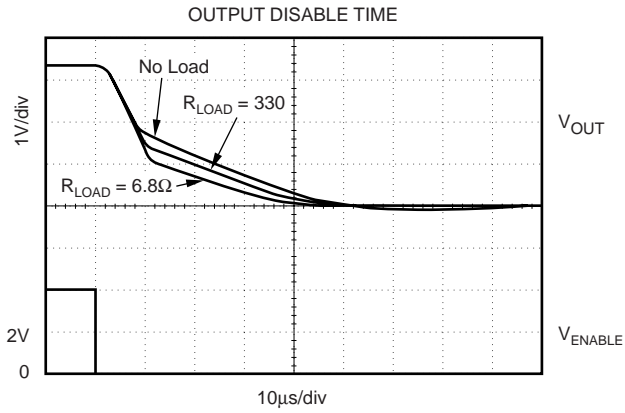
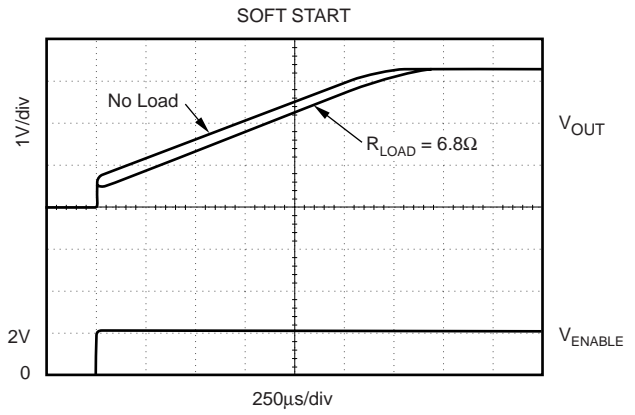
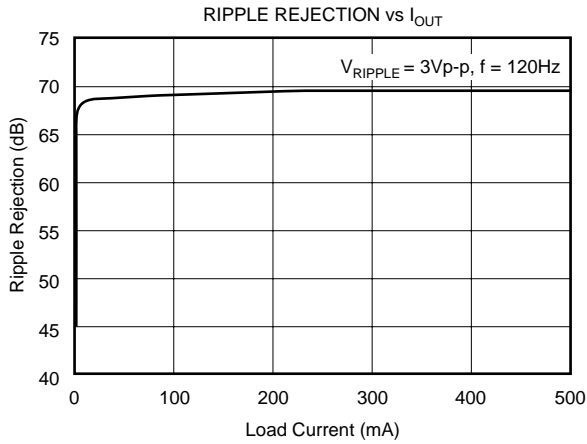
# TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 2\text{V}$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 2\text{V}$ , unless otherwise noted.





## BASIC OPERATION

The REG103 series is a family of LDO (Low Drop-Out) linear regulators. The family includes five fixed output versions (2.5V to 5.0V) and an adjustable output version. An internal DMOS power device provides low dropout regulation with near constant ground pin current (largely independent of load and drop-out conditions) and very fast line and load transient response. All versions include internal current limit and thermal shutdown circuitry.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG103A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2. The SO-8 package provides two pins each for  $V_{IN}$  and  $V_{OUT}$ . Both sets of pins **MUST** be used and connected adjacent to the device.

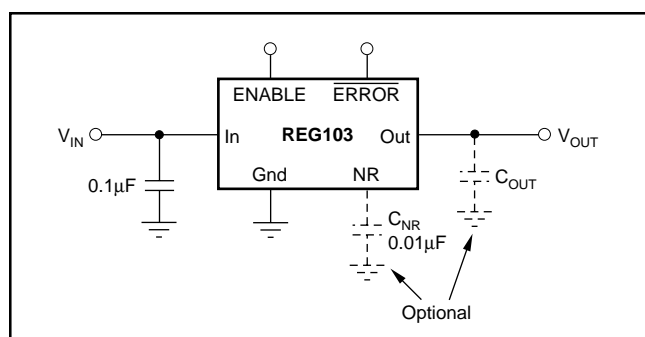


FIGURE 1. Fixed Voltage Nominal Circuit for REG103.

None of the versions require an output capacitor for regulator stability. The REG103 will accept any output capacitor type less than 1µF. For capacitance values larger than 1µF, the effective ESR should be greater than 0.1Ω. This minimum ESR value includes parasitics such as printed circuit board traces, solder joints, and sockets. A minimum 0.1µF low ESR capacitor connected to the input supply voltage is recommended.

### INTERNAL CURRENT LIMIT

The REG103 internal current limit has a typical value of 700mA. A fold-back feature limits the short-circuit current to a typical short-circuit value of 40mA. This circuit will protect the regulator from damage under all load conditions. A typical characteristic of  $V_{OUT}$  versus  $I_{OUT}$  is given in Figure 3a.

Care should be taken in high current applications to avoid ground currents flowing in the circuit board traces causing voltage drops between points on the circuit. If voltage drops occur on the circuit board ground that causes the load ground voltage to be much lower than the ground voltage seen by the ground pin on the REG103, the foldback current may approach zero and the REG103 may not start up. In these types of applications, a large value resistor can be placed between  $V_{IN}$  and  $V_{OUT}$  to help “boost” up the output of the REG103 during start-up, see Figure 3b. The value for the “boost” resistor should be chosen so that the current through the “boost” resistor is less than the minimum load current:  $R_{BOOST} > (V_{IN} - V_{OUT})/I_{LOAD}$ . Typically, a good value for a “boost” resistor is 5kΩ.

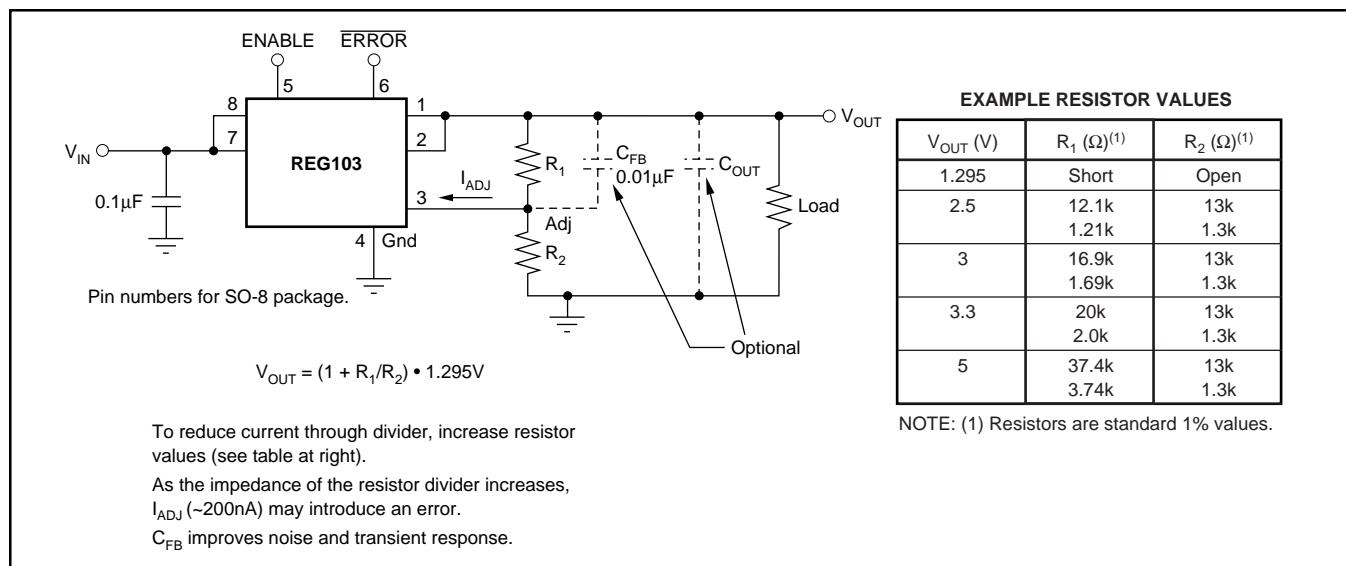


FIGURE 2. Adjustable Voltage Circuit for REG103A.

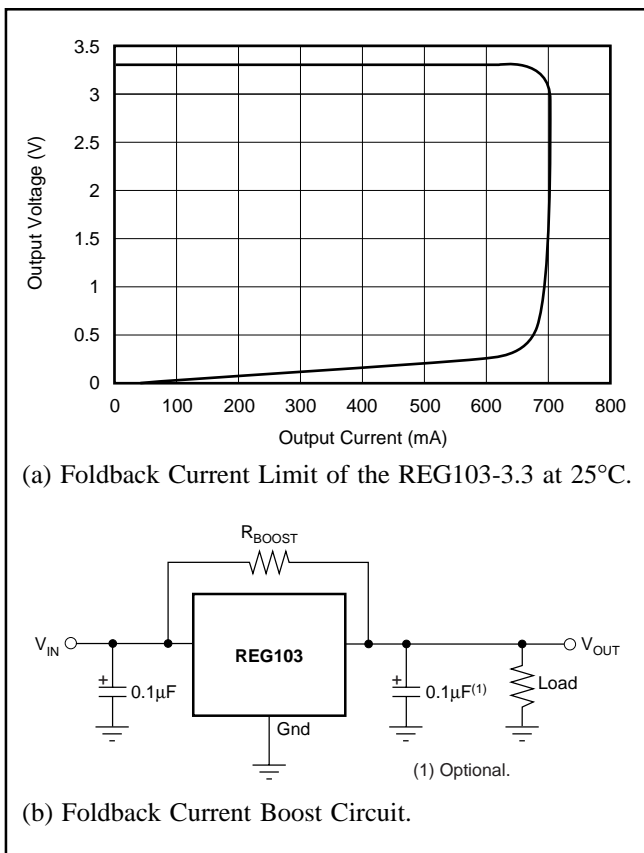


FIGURE 3. Foldback Current Limit and Boost Circuit.

## ENABLE

The ENABLE pin allows the regulator to be turned on and off. This pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 0.5μA. When not used, the ENABLE pin may be connected to V<sub>IN</sub>.

Internal to the part, the ENABLE pin is connected to an input resistor-zener diode circuit, as shown in Figure 4, creating a nonlinear input impedance. The ENABLE Pin Current versus Applied Voltage relationship is shown in Figure 5. When the ENABLE pin is connected to a voltage greater than 10V, a series resistor may be used to limit the current.

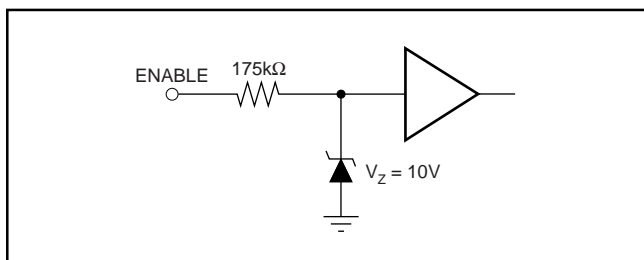


FIGURE 4. ENABLE Pin Equivalent Input Circuit.

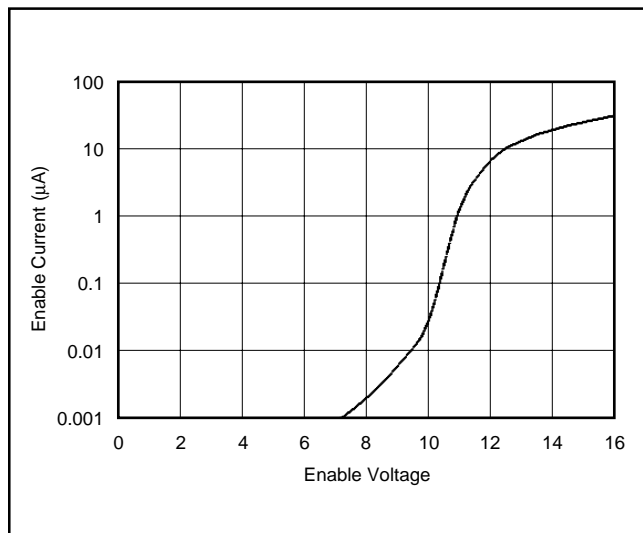


FIGURE 5. ENABLE Pin Current versus Applied Voltage.

## ERROR FLAG

The error indication pin, only available on the SO-8 package version, provides a fault indication out-of-regulation condition. During a fault condition,  $\overline{\text{ERROR}}$  is pulled LOW by an open drain output device. The pin voltage, in the fault state, is typically less than 0.2V at 500μA.

A fault condition is indicated when the output voltage differs (either above or below) from the specified value by approximately 10%. Figure 6 shows a typical fault-monitoring application.

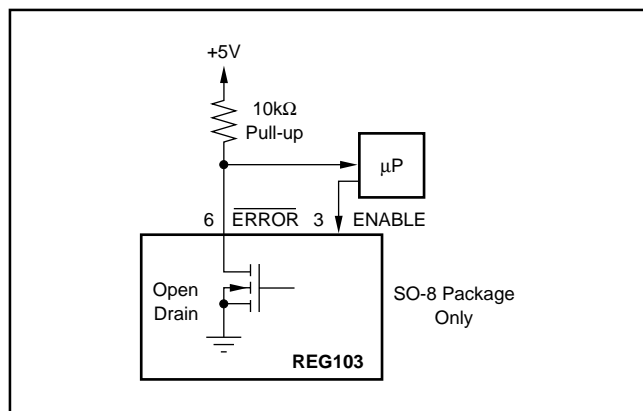


FIGURE 6.  $\overline{\text{ERROR}}$  Pin Typical Fault-Monitoring Circuit.

## OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage, V<sub>REF</sub>, for the REG103. This reference is the dominant noise source within the REG103. It generates approximately 45μVrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 45\mu\text{Vrms} \frac{R_1 + R_2}{R_2} = 45\mu\text{Vrms} \cdot \frac{V_{\text{OUT}}}{V_{\text{REF}}}$$

Since the value of  $V_{REF}$  is 1.295V, this relationship reduces to:

$$V_N = 35 \frac{\mu V_{rms}}{V} \bullet V_{OUT}$$

Connecting a capacitor,  $C_{NR}$ , from the Noise-Reduction (NR) pin to ground, can reduce the output noise voltage. Adding  $C_{NR}$ , as shown in Figure 7, forms a low-pass filter for the voltage reference. For  $C_{NR} = 10nF$ , the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 3.5, as shown in Figure 8.

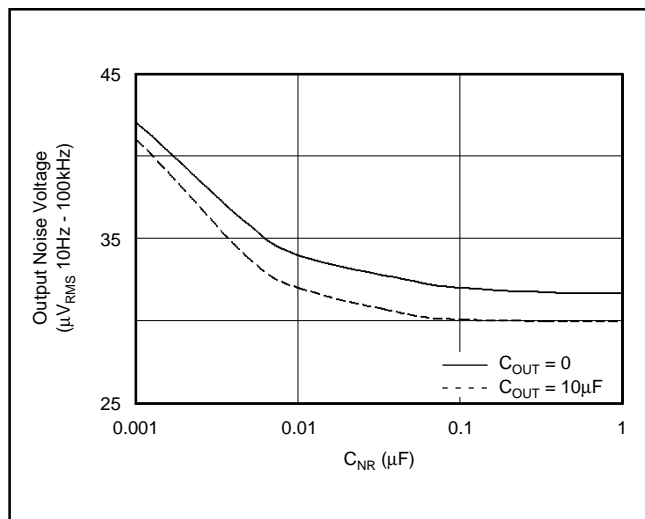


FIGURE 8. Output Noise versus Noise-Reduction Capacitor.

The REG103 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor,  $C_{FB}$ , connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. Figure 9 shows improved output noise performance for two capacitor combinations.

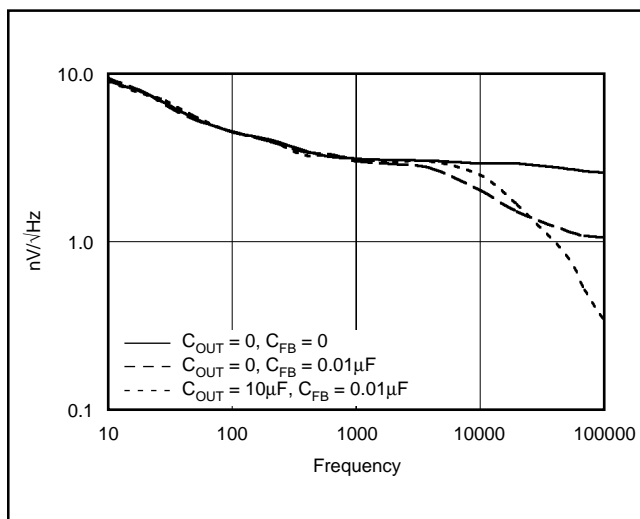


FIGURE 9. Output Noise Density on Adjustable Versions.

The REG103 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above  $V_{IN}$ . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator.

## DROP-OUT VOLTAGE

The REG103 uses an N-channel DMOS as the “pass” element. When the input voltage is within a few hundred millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of  $V_{IN}$  to  $V_{OUT}$ , the regulator’s input-to-output resistance is the  $R_{DS(ON)}$  of the DMOS pass element (typically 230mΩ). For static (DC) loads, the REG103 will typically maintain regulation down to  $V_{IN}$  to  $V_{OUT}$  voltage drop of 115mV at full-rated output current. In Figure 10, the bottom line (DC dropout) shows the minimum  $V_{IN}$  to  $V_{OUT}$  voltage drop required to prevent drop-out under DC load conditions.

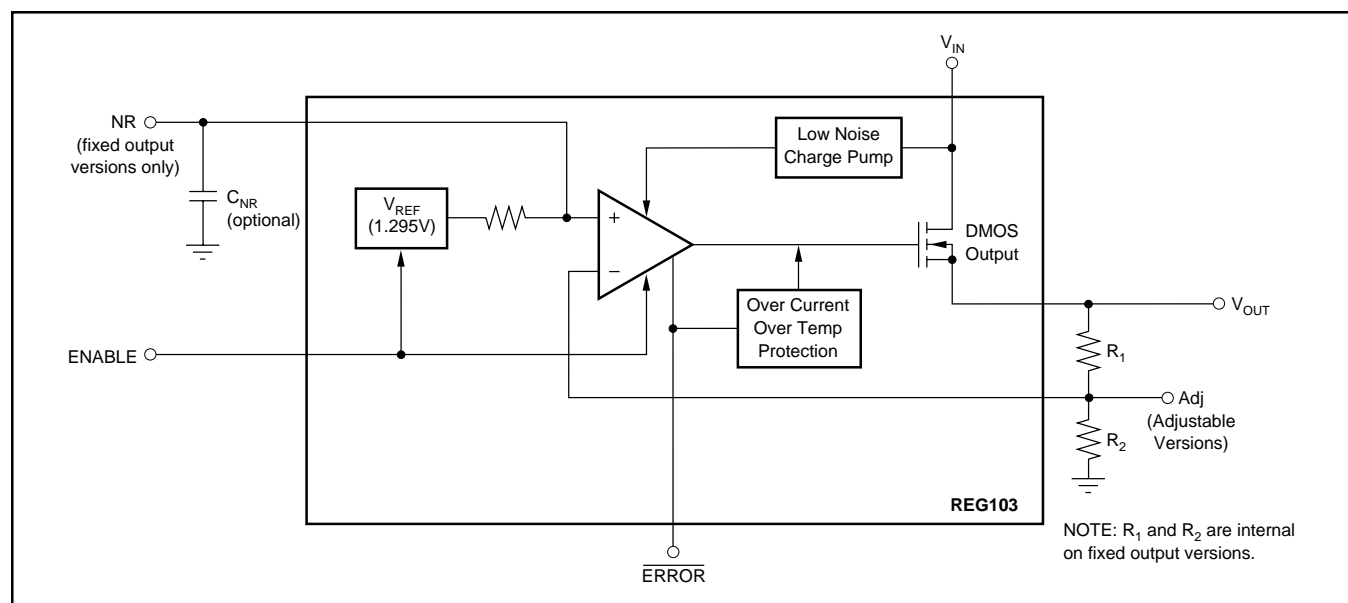


FIGURE 7. Block Diagram.

For large step changes in load current, the REG103 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this “transient drop-out” region is shown as the top line in Figure 10. Values of  $V_{IN}$  to  $V_{OUT}$  voltage drop above this line insure normal transient response.

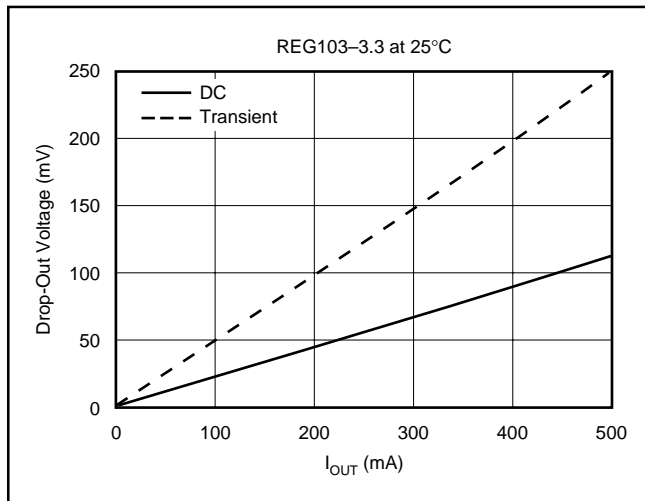


FIGURE 10. Transient and DC Dropout.

In the transient dropout region between “DC” and “Transient”, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available “headroom”  $V_{IN}$  to  $V_{OUT}$  voltage drop. Under worst-case conditions (full-scale load change with  $V_{IN}$  to  $V_{OUT}$  voltage drop close to DC dropout levels), the REG103 can take several hundred microseconds to re-enter the specified window of regulation.

## TRANSIENT RESPONSE

The REG103 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 10nF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor,  $C_{FB}$  (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

## THERMAL PROTECTION

Power dissipated within the REG103 will cause the junction temperature to rise. The REG103 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 150°C, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be

limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG103 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG103 into thermal shutdown will degrade reliability.

## POWER DISSIPATION

The REG103 is available in three different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit-board layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult-to-impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 11. In all cases, the PCB copper area is bare copper, free of solder-resist mask, and not solder plated. All examples are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

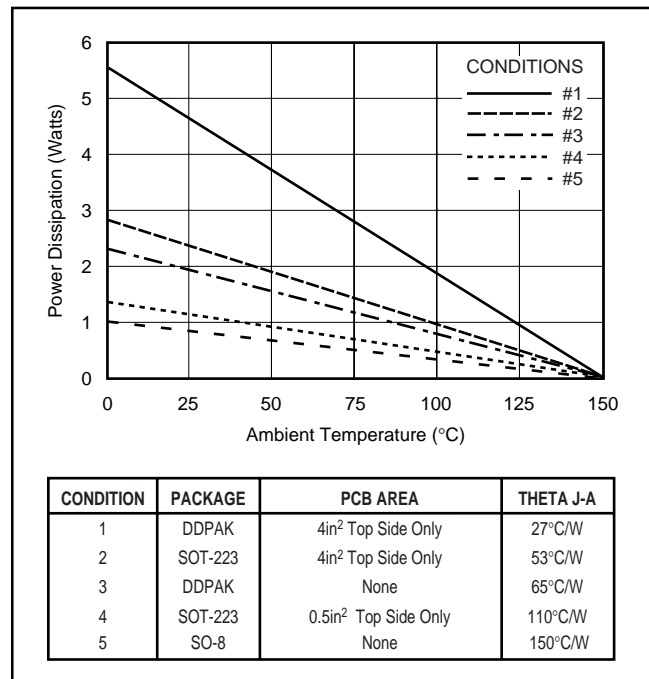


FIGURE 11. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the average output current times the voltage across the output element,  $V_{IN}$  to  $V_{OUT}$  voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

## REGULATOR MOUNTING

The tab of both packages is electrically connected to ground. For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit-

board copper area. Increasing the copper area improves heat dissipation. Figure 12 shows typical thermal resistance from junction to ambient as a function of the copper area for the DDPAK.

Although the tabs of the DDPAK and the SOT-223 are electrically grounded, they are not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG103 devices are presented in the Application Bulletin “Solder Pad Recommendations for Surface-Mount Devices” (SBFA015), available from the Texas Instruments web site ([www.ti.com](http://www.ti.com)).

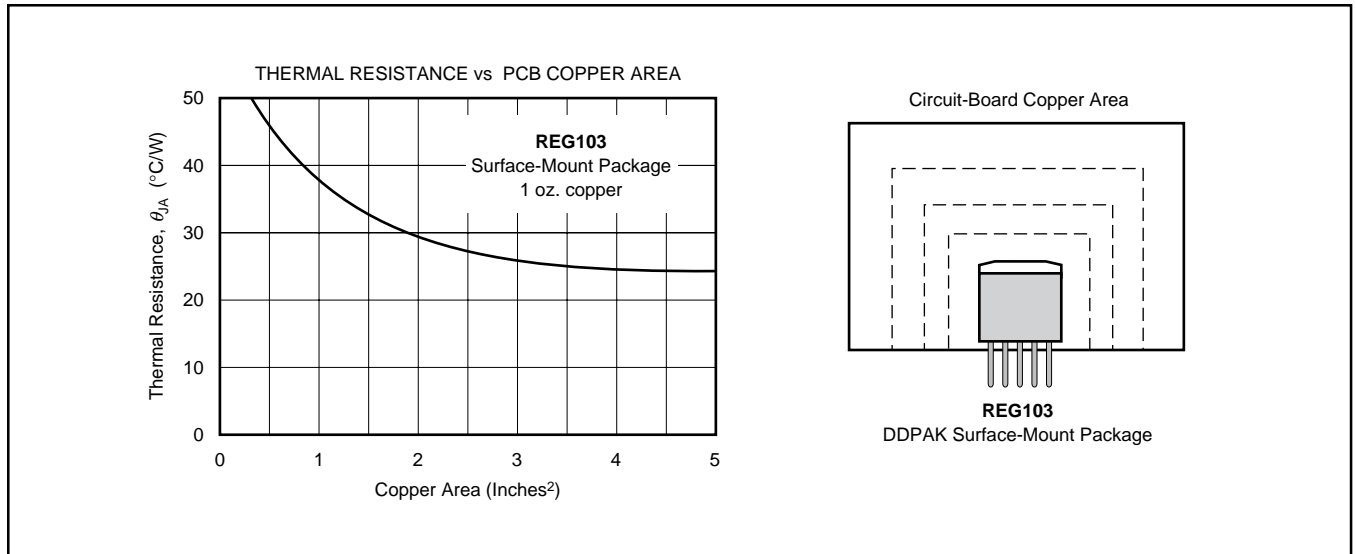


FIGURE 12. Thermal Resistance versus PCB Area for the Five-Lead DDPAK.

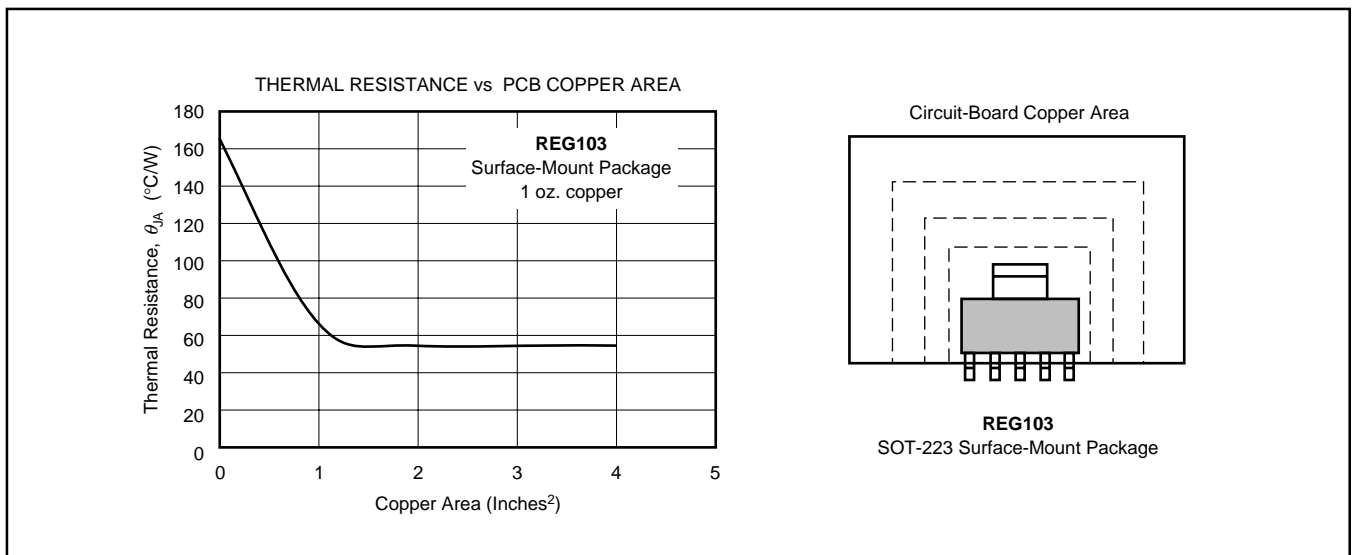
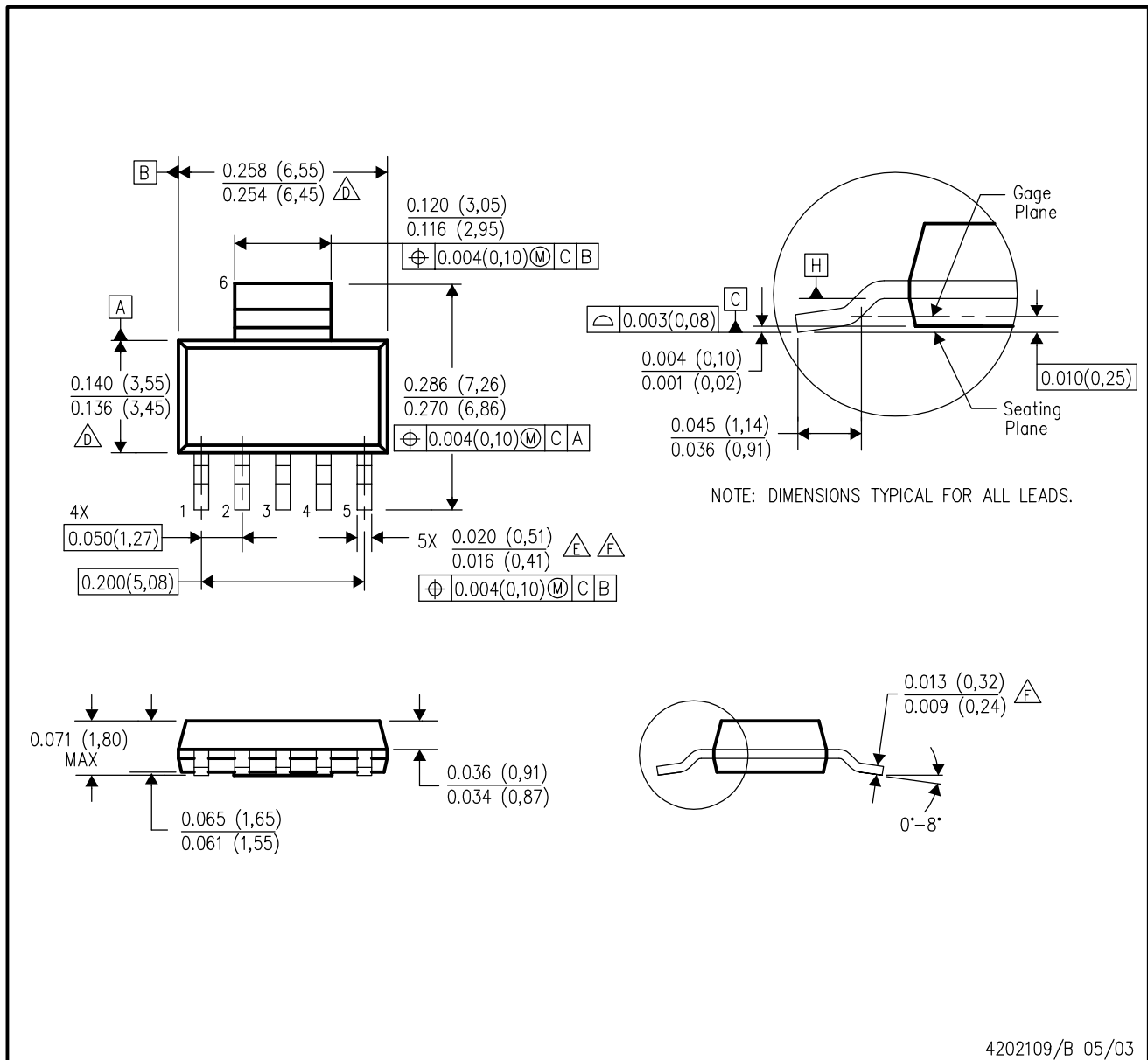


FIGURE 13. Thermal Resistance versus PCB Area for the Five-Lead SOT-223.

DCQ (R-PDSO-G6)

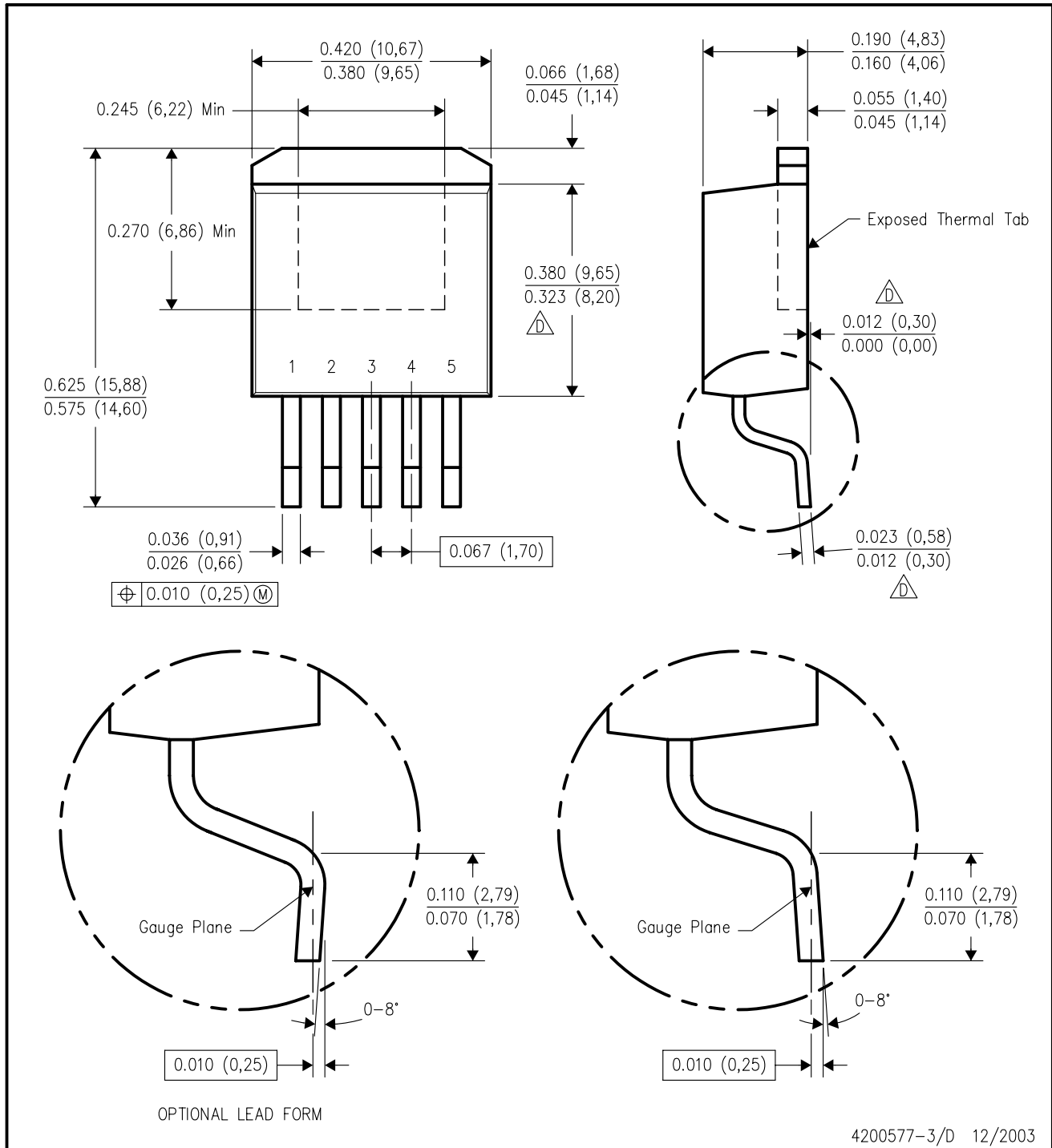
PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Controlling dimension in inches.
  - $\triangle D$  Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
  - $\triangle E$  Lead width dimension does not include dambar protrusion.
  - $\triangle F$  Lead width and thickness dimensions apply to solder plated leads.
  - G. Interlead flash allow 0.008 inch max.
  - H. Gate burr/protrusion max. 0.006 inch.
  - I. Datums A and B are to be determined at Datum H.
  - J. Package dimensions per JEDEC outline drawing TO-261, issue B, dated Feb. 1999. This variation is not yet included.

KTT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE

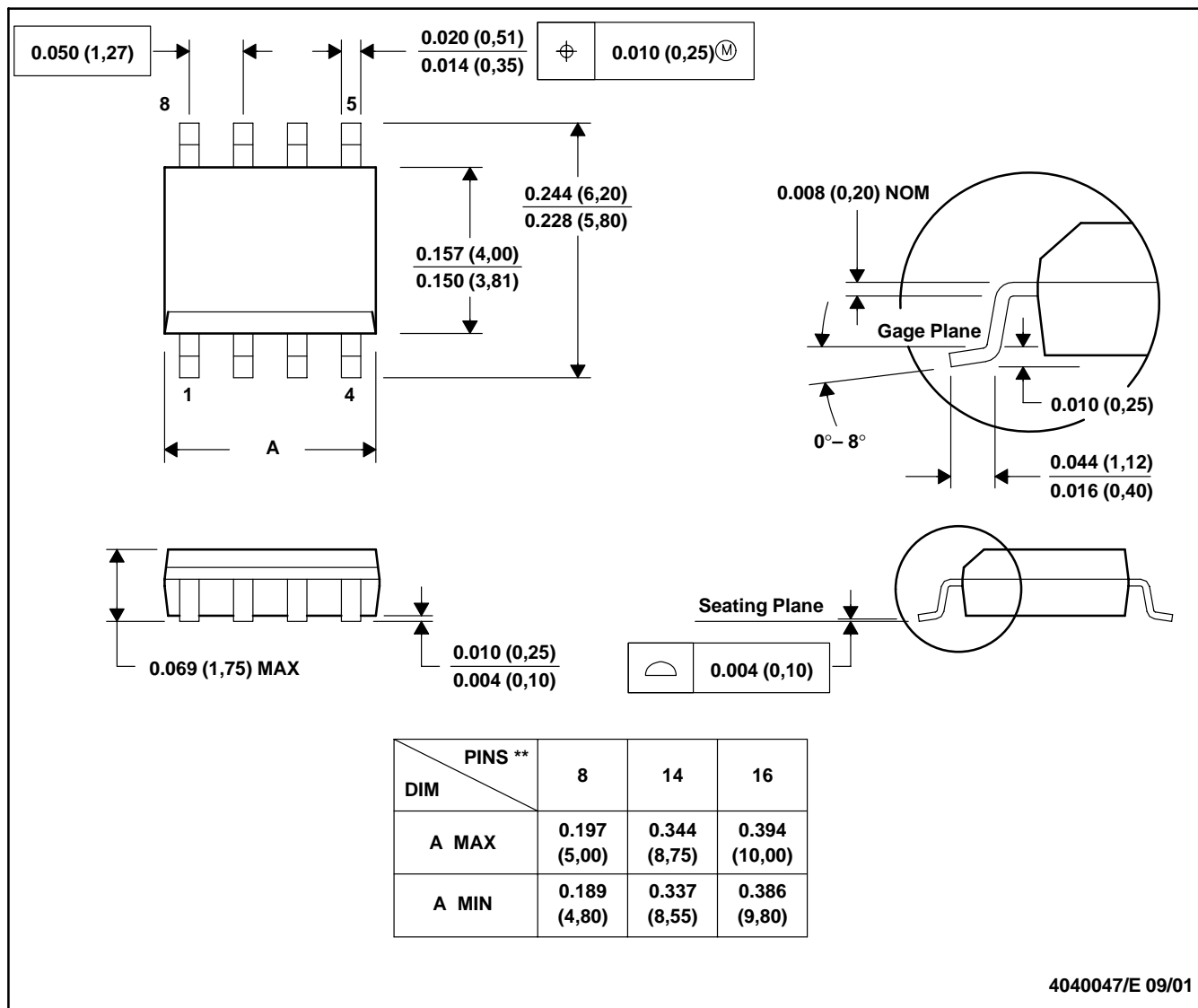


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
- △ Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012



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