EPSON®

S1D13505 Embedded RAMDAC LCD/CRT Controller

Power Consumption

Document Number: X23A-G-006-03

THIS PAGE LEFT BLANK

1 S1D13505 Power Consumption

S1D13505 power consumption is affected by many system design variables.

- Input clock frequency (CLKI): the CLKI frequency determines the LCD frame-rate, CPU performance to memory, and other functions – the higher the input clock frequency, the higher the frame-rate, performance and power consumption.
- CPU interface: the S1D13505 current consumption depends on the BUSCLK frequency, data width, number of toggling pins, and other factors – the higher the BUSCLK, the higher the CPU performance and power consumption.
- V_{DD} voltage level: the voltage level affects power consumption – the higher the voltage, the higher the consumption.
- Display mode: the resolution and color depth affect power consumption – the higher the resolution/color depth, the higher the consumption.
- Internal CLK divide: internal registers allow the input clock to be divided before going to the internal logic blocks – the higher the divide, the lower the power consumption.

There are two power save modes in the S1D13505: Software and Hardware SUSPEND. The power consumption of these modes is affected by various system design variables.

- DRAM refresh mode (CBR or self-refresh): self-refresh capable DRAM allows the S1D13505 to disable the internal memory clock thereby saving power.
- CPU bus state during SUSPEND: the state of the CPU bus signals during SUSPEND has a substantial effect on power consumption. An inactive bus (e.g. BUSCLK = low, Addr = low etc.) reduces overall system power consumption.
- CLKI state during SUSPEND: disabling the CLKI during SUSPEND has substantial power savings.

1.1 Conditions

Table 1-1: "S1D13505 Total Power Consumption" below gives an example of a specific environment and its effects on power consumption.

Table 1-1: S1D13505 Total Power Consumption

	Test Condition V_{DD} = 3.3V ISA Bus (8MHz)	Gray Shades / Colors	Total Power Consumption		
			Active	Power Save Mode	
				Software	Hardware
1	Input Clock = 6MHz LCD Panel = 320x240 4-bit Single Monochrome	Black-and-White 4 Gray Shades 16 Gray Shades	18.6mW 20.3mW 22.8mW	4.29mW[1]	0.33µW[2]
2	Input Clock = 6MHz LCD Panel = 320x240 8-bit Single Color	4 Colors 16 Colors 256 Colors	22.3mW 25.3mW 29.0mW	4.32mW[1]	0.33µW[2]
3	Input Clock = 25MHz LCD Panel = 640x480 8-bit Dual Monochrome	Black-and-White 16 Gray Shades	58.5mW 71.7mW	5.71mW[1]	0.33µW[2]
4	Input Clock = 25MHz LCD Panel = 640x480 16-bit Dual Color	16 Colors 256 Colors 64K Colors	93.4mW 98.1mW 101.3mW	5.74mW[1]	0.33µW[2]
5	Input Clock = 33.333MHz CRT = 640x480 Color	16 Colors 256 Colors 64K Colors	221.1mW 234.0mW 237.3mW	6.34mW[1]	0.33µW[2]

Note

1. Conditions for Software SUSPEND:
   - CPU interface active (signals toggling)
   - CLKI active
   - Self-Refresh DRAM

2. Conditions for Hardware SUSPEND:
   - CPU interface inactive (high impedance)
   - CLKI stopped
   - Self-Refresh DRAM

2 Summary

The system design variables in Section 1, "S1D13505 Power Consumption" and in Table 1-1: "S1D13505 Total Power Consumption" show that S1D13505 power consumption depends on the specific implementation. Active Mode power consumption depends on the desired CPU performance and LCD frame-rate, whereas Power Save Mode consumption depends on the CPU Interface and Input Clock state.

In a typical design environment, the S1D13505 can be configured to be an extremely power-efficient LCD Controller with high performance and flexibility.